



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/073,495	02/11/2002	William A. Stevens, JR.	042390.P9143	6012
7590	01/04/2008			
Lawrence E. Lycke BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP Seventh Floor 12400 Wilshire Boulevard Los Angeles, CA 90025-1026			EXAMINER CHEN, TSE W	
			ART UNIT 2116	PAPER NUMBER
			MAIL DATE 01/04/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

mh

Office Action Summary	Application No.	Applicant(s)
	10/073,495	STEVENS, ET AL.
	Examiner	Art Unit
	Tse Chen	2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 31 October 2007.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 42-56 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 42-56 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 31, 2007 has been entered.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: “computer-readable medium” of claims 50-53 should be “computer-readable storage medium” to correlate with the subject matter disclosed in paragraph 0072 of the specification.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 42-44, 48, 50-51, 53-56 are rejected under 35 U.S.C. 102(b) as being anticipated by Datta, US Patent 6081890.

5. In re claim 42, Datta discloses a method comprising:

- Executing a core module [bootstrap] [col.1, ll.29-30].

Art Unit: 2116

- Initializing a plurality of firmware modules [procedures, routines] by the core module [col.1, ll.21-24, ll.28-31], wherein the initializing comprises:
 - Examining at least two firmware modules [e.g., checking integrity of memory, identifying and initializing other resources] to determine a required order of dispatch of the firmware modules [col.1, ll.31-34].
 - Dispatching an earlier of the two firmware modules by the core module and then dispatching a later of the two firmware modules by the core module [col.1, ll.31-34; e.g., check integrity before initialization].
 - After initializing the plurality of firmware modules, initializing a system memory [volatile] [col.1, ll.15-18].
- Invoking a function [legacy firmware dispatcher] contained in a third firmware module [legacy firmware] by the earlier of the two firmware modules [native firmware] during a dispatch of the earlier firmware module or by the later of the two firmware modules during a dispatch of the later firmware module [col.6, ll.35-39].

6. In re claim 43, Datta discloses, wherein examining comprises checking a resource list [components] of each of the two firmware modules [col.4, ll.1-3].

7. In re claim 44, Datta discloses, wherein the initializing of the plurality of firmware modules comprises determining the requirements configuration of the plurality of firmware modules appropriate to run [col.1, l.45] and examining a platform to determine [identify] whether hardware to be initialized by the module is present in the platform [col.1, ll.31-32].

8. As to claim 48, Datta discloses, wherein the third firmware module is dispatched before the function contained in the third firmware module is invoked [col.6, ll.35-39].

Art Unit: 2116

9. In re claim 50, Datta discloses each and every limitation as discussed above in reference to claim 42. Datta discloses a computer-readable medium containing instructions to cause a programmable processor to perform operations [col.10, l.13] comprising determining dependencies among a plurality of firmware modules by a separate core module based on information about services imported and exported by each of the firmware modules before dispatching the plurality of firmware modules by the separate core module, and the services imported by each firmware module of the plurality of firmware modules dispatched by the separate core module are provided in another firmware of the plurality of firmware modules dispatched by the separate core module [col.2, ll.1-6; col.3, ll.60-67; implicitly, IA64 depends on IA32 legacy resources].

10. As to claim 51, Datta discloses an import table [242] comprising at least one service that may be called by the firmware module.

11. As to claim 53, Datta discloses, wherein dispatching a module comprises saving a return address in a processor register [radd] and executing a beginning instruction of the module [col.4, ll.17-20].

12. In re claim 54, Datta discloses each and every limitation as discussed above in reference to claim 42. Datta discloses a system comprising one of the two firmware modules is to initialize a hardware component that is not present in the system by iterating through each of the plurality of firmware modules within the BIOS [col.3, l.34] to determine whether the hardware component is present [col.1, ll.56-67; IA-32 processors not present].

13. As to claim 55, Stevens discloses, wherein the volatile memory is a RAM [col.1, ll.35-36].

14. As to claim 56, Stevens discloses, wherein the non-volatile memory is at least one of a ROM or a flash memory [col.3, ll.20-22].

15. Claims 45-47, 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Datta as applied to claim 42 above, and further in view of Ayers et al., US Patent 6353924, hereinafter Ayers.

16. Datta taught each and every limitation of the claim as discussed above. Datta did not disclose explicitly marking a data structure after dispatching a firmware module.

17. In re claim 45, Ayers discloses a method comprising marking a data structure [e.g., table] after dispatching a firmware module [e.g., block], wherein the data structure is to indicate whether the firmware module has been dispatched [col.4, ll.51-58].

18. It would have been obvious to one of ordinary skill in the art, having the teachings of Ayers and Datta before him at the time the invention was made, to modify the system taught by Datta to include the explicit well known data structure teachings of Ayers, as using data structures to record an event [e.g., dispatched firmware module] is very well known and suitable for use in the system of Datta. One of ordinary skill in the art would have been motivated to make such a combination as it provides a very well known way to record events and aid debugging efforts [Ayers: col.1, ll.1-30].

19. As to claim 46, Ayers discloses, wherein the data structure is a bit array [circular buffer] [col.4, ll.17-19].

20. As to claim 47, Ayers discloses, wherein the data structure is held in a processor register [col.4, ll.5-16].

Art Unit: 2116

21. As to claim 52, Ayers discloses each and every limitation as discussed above in reference to claims 45 and 47.

22. Claim 49 is rejected under 35 U.S.C. 103(a) as being unpatentable over Datta as applied to claim 48 above, and further in view Katayama et al., US Publication 20010007119, hereinafter Katayama.

23. Datta taught each and every limitation of the claim as discussed above. Datta discloses scanning to find a module that operates with a hardware component present in the platform and invoking the function if such a module is found [col.1, ll.31-33]. Datta did not disclose explicitly did not disclose explicitly the firmware modules being arranged in a daisy chain.

24. Katayama discloses a method comprises a daisy chain of [firmware] modules [e.g., 85, 91] [0107-0109].

25. It would have been obvious to one of ordinary skill in the art, having the teachings of Datta and Katayama before him at the time the invention was made, to modify the system taught by Datta to include the explicit well known daisy chain teachings of Katayama, as using daisy chains to organize related objects [e.g., firmware module] is very well known and suitable for use in the system of Datta. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to organize data that allows continuous access without the data being required to be stored in a continuous location [Katayama: 0109].

Response to Arguments

26. Applicant's arguments filed October 31, 2007 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Art Unit: 2116

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Tse Chen
January 1, 2008